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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/531,757	04/14/2005	Thierry Sicard	SC12366ET	2223	
	23125 7590 03/18/2008 FREESCALE SEMICONDUCTOR, INC.			EXAMINER	
LAW DEPARTMENT			LAM, TUAN THIEU		
AUSTIN, TX 7	ARMER LANE MD:TX32/PL02 78729		ART UNIT	PAPER NUMBER	
			2816		
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			03/18/2008	PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)
	10/531,757	SICARD, THIERRY
Office Action Summary	Examiner	Art Unit
	Tuan T. Lam	2816
The MAILING DATE of this communication ap Period for Reply	ppears on the cover sheet with the c	orrespondence address
A SHORTENED STATUTORY PERIOD FOR REPL WHICHEVER IS LONGER, FROM THE MAILING ID. - Extensions of time may be available under the provisions of 37 CFR 1 after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period. - Failure to reply within the set or extended period for reply will, by statuly Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	DATE OF THIS COMMUNICATION 136(a). In no event, however, may a reply be tind will apply and will expire SIX (6) MONTHS from te, cause the application to become ABANDONE	N. nely filed the mailing date of this communication. D (35 U.S.C. § 133).
Status		
Responsive to communication(s) filed on 17. This action is FINAL . 2b) ☐ This action is FINAL . Since this application is in condition for allowated closed in accordance with the practice under	is action is non-final. ance except for formal matters, pro	
Disposition of Claims		
4) Claim(s) 1 and 3-16 is/are pending in the app 4a) Of the above claim(s) is/are withdra 5) Claim(s) 1,3-6,8-10,12-14 and 16 is/are allow 6) Claim(s) 7,11 and 15 is/are rejected. 7) Claim(s) is/are objected to. 8) Claim(s) are subject to restriction and/	awn from consideration. red.	
9) The specification is objected to by the Examin 10) The drawing(s) filed on is/are: a) ac Applicant may not request that any objection to the Replacement drawing sheet(s) including the correct 11) The oath or declaration is objected to by the E	cepted or b) objected to by the lead of a drawing(s) be held in abeyance. Section is required if the drawing(s) is objection	e 37 CFR 1.85(a). jected to. See 37 CFR 1.121(d).
Priority under 35 U.S.C. § 119		
12) Acknowledgment is made of a claim for foreig a) All b) Some * c) None of: 1. Certified copies of the priority documer 2. Certified copies of the priority documer 3. Copies of the certified copies of the priority application from the International Burea * See the attached detailed Office action for a list	nts have been received. nts have been received in Applicationity documents have been received au (PCT Rule 17.2(a)).	on No ed in this National Stage
Attachment(s)	4) 🗖 Interview Commerce	(PTO 413)
 Notice of References Cited (PTO-892) Notice of Draftsperson's Patent Drawing Review (PTO-948) Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 	4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal F 6) Other:	ate

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DETAILED ACTION

This is a response to the amendment filed 1/17/2008. Claims 1 and 3-16 are under examination.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 2. Claims 7, 11 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Umemoto (USP 6,448,752).

Figure 1 shows a transmitter for a controlled shape switched signal (output of transistor Q) on a communication line (electrical wire connected to the transistor Q) comprising signal generator means including capacitor means (Ca), and signal producing means (Q) responsive to a capacitor voltage (voltage at node 131) across said capacitor means for applying said switched signal to said line, and charging means (2-5) responsive to an input signal (VIN) for supplying a charging current (I in 4) to said capacitor means so as to define an edge of said switched signal, characterized in that said charging means comprises feedback loop means responsive to said capacitor voltage for generating a feedback current (current along collector emitter path of transistor Q8) having a continuous magnitude that is progressive function of said capacitor voltage (the feedback current provides a continuous current when the switch Q8 is on, switch Q8 is responsive to the capacitor voltage via comparators 3a, 3b and RS flip flop 3c), said charging current being a function of said feedback current (the current I changes when Q8 is on, thus,

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charging current I is function of the feedback current) so that the range of change of said capacitor voltage is a continuous function of time (the rate of change of the capacitor voltage at node 131 is Vo = 1/Ca \int I dt which is a continuous function), wherein said charging means is selectively responsive to said input signal for supplying a positive or a negative charging current to said capacitor means, whereby to generate a rising or a falling edge of said switched signal (charging current producing circuit 4 produces a charging current, i.e., increasing or decreasing, dependent upon the amplitude value of the input signal (column 3, lines 1-25), to the capacitor means, thus, defining the falling or rising edge of the switched signal generated by the transistor Q) as called for in claim 7.

Regarding claim 11, the capacitor voltage varies substantially as a sinusoidal half cycle having a single frequency to define said edge of said switched signal (the capacitor voltage $Vo = 1/Ca \int I \, dt$ varies as a sinusoidal wave with half cycle determined by the charging current, the sinusoidal wave has a frequency defined the edge of said switched signal).

Regarding claim 15, wherein the charging means comprises resistive means (transistor Q8 inherently has resistive quantity) for receiving a voltage that is a function of said capacitor voltage (via the comparators 3a, 3b and 3c) for generating a feedback current.

Allowable Subject Matter

3. Claims 1, 3-6, 8-10, 12-14 and 16 are presently allowed.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. In this regard, applicant's cited prior art have been carefully considered.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 571-272-1744. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richard can be reached on 571-272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Tuan T. Lam/ Primary Examiner Art Unit 2816

2/29/2008